

CLAIMS

We claim:

1           1.    A programmable logic device comprising:  
2           input/output buffers adapted to programmably support a  
3 plurality of signal types;  
4           a serializer deserializer circuit adapted to receive a  
5 serial input data stream and extract a clock and provide a  
6 parallel data output signal and further adapted to receive a  
7 parallel data input signal and provide a serial output data  
8 stream; and  
9           a programmable interconnect adapted to selectively couple  
10 the input/output buffers to the serializer deserializer circuit.

1           2.    The programmable logic device of Claim 1, wherein the  
2 programmable interconnect couples the input/output buffers to  
3 the serializer deserializer circuit to route signals through the  
4 serializer deserializer circuit when the signals exceed a clock  
5 rate of a core logic of the programmable logic device, and  
6 decouples the input/output buffers from the serializer  
7 deserializer circuit to bypass the serializer deserializer  
8 circuit when the signals are within the clock rate of the core  
9 logic.

1           3.    The programmable logic device of Claim 1, wherein the  
2 signal types include LVTTTL, LVCMOS, PCI, PCI-X, SSTL, HSTL,  
3 GTL+, CTT, BLVDS, LVDS, and LVPECL.

1           4.    The programmable logic device of Claim 1, wherein the  
2   serializer deserializer circuit comprises:  
  
3           a first receiver having a deserializer and a clock and data  
4   recovery function;  
  
5           a first transmitter, associated with the first receiver,  
6   having a serializer function;  
  
7           a second receiver having a deserializer and a clock and  
8   data recovery function; and  
  
9           a second transmitter, associated with the second receiver,  
10   having a serializer function.

1           5.    The programmable logic device of Claim 4, wherein the  
2   serializer deserializer circuit further comprises a phase-locked  
3   loop circuit adapted to provide a high speed clock for the  
4   serializer deserializer circuit.

1           6.    The programmable logic device of Claim 5, wherein the  
2   programmable interconnect couples the input/output buffers to  
3   the serializer deserializer circuit when high speed serial data  
4   transfer capability is required over differential signal  
5   input/output paths.

1           7.    The programmable logic device of Claim 1, further  
2   comprising a memory, the programmable interconnect selectively  
3   couples the memory to the input/output buffers.

1           8.     The programmable logic device of Claim 7, wherein the  
2 memory provides synchronization support.

1           9.     The programmable logic device of Claim 7, wherein the  
2 memory comprises RAM, ROM, FIFO, single-port, or dual-port  
3 memory.

1           10.    A programmable interface circuit, within a  
2 programmable logic device, comprising:  
  
3           input/output buffers adapted to support a number of  
4 input/output signal types;  
  
5           means for providing serializer/deserializer and clock and  
6 data recovery; and  
  
7           means for programmably coupling the providing means to the  
8 input/output buffers for high-speed serial signal streams  
9 transferred through the input/output buffers which exceed a core  
10 clock rate of the programmable logic device.

1           11.    The programmable interface circuit of Claim 10,  
2 wherein the input/output signal types include single-ended  
3 signals and differential signals.

1           12.    The programmable interface circuit of Claim 10,  
2 further comprising a memory, wherein the coupling means  
3 programmably couples the memory to the input/output buffers to  
4 provide synchronization functions.

1        13. The programmable interface circuit of Claim 12,  
2 wherein the coupling means decouples the providing means from  
3 the input/output buffers and routes signals transferred through  
4 the input/output buffers between the input/output buffers and  
5 the memory or a core logic of the programmable logic device when  
6 a rate of the signals is within the core clock rate.

1        14. The programmable interface circuit of Claim 13,  
2 wherein the core logic implements logic, memory, arithmetic, or  
3 register functions.

1        15. The programmable interface circuit of Claim 10,  
2 wherein the providing means comprises a pair of serializer  
3 deserializer circuits and a phase-locked loop.

1        16. The programmable interface circuit of Claim 10,  
2 wherein the coupling means comprises a pair of input/output  
3 blocks and a switch matrix.

1        17. A method of providing a programmable interface for a  
2 programmable logic device, the method comprising:

3        providing buffers adapted to programmably transfer a number  
4 of different signal types to and from the programmable logic  
5 device; and

6        providing a programmable interconnect to selectively couple  
7 or decouple an interface circuit, having serializer,

8 deserializer, and clock and data recovery capability, to the  
9 buffers depending upon the signal type.

1 18. The method of Claim 17, wherein the signal types  
2 comprise single-ended signals and differential signals.

1 19. The method of Claim 18, wherein the programmable  
2 interconnect couples the interface circuit to the buffers when  
3 the signal type is a differential signal that exceeds a core  
4 clock rate of the programmable logic device, and decouples the  
5 interface circuit when the signal type does not exceed the core  
6 clock rate.

1 20. The method of Claim 19, further comprising providing  
2 memory adapted to programmably couple to the programmable  
3 interconnect.